ABSTRACT OF THE DISCLOSURE

A shift-register circuit comprises an inverter and first to fourth transistors. The first transistor includes a gate coupled to an inverse clock signal, and a first source/drain coupled to a signal output from a previous-stage shift-register unit. The inverter includes a first input terminal coupled to the first source/drain of the first transistor. The second transistor includes a gate coupled to a second source/drain of the first transistor, a first source/drain coupled to a clock signal, and a second source/drain coupled to an output terminal. The third transistor includes a gate coupled to a first output terminal of the inverter, a first source/drain coupled to the output terminal, and a second source/drain coupled to a first voltage. The fourth transistor includes a gate coupled to a signal output from a next-stage shift-register unit, a first source/drain coupled to the output terminal, and a second source/drain coupled to the first voltage.